EDSFF-E1.S GEN5 BP
USER'S MANUAL

P/N : 2RAKVI016400

Model：1U08-EDSFF-E1S BP-H -GEN5 MODULE

Version: V1.0

Revision History

Version	Changes	Date
V1.0	Official Release	2024/05/10

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Overview

The backplane is a high performance economical solution for users who has sufficient MCIO host ports on MB or RAID/HBA to accommodate 8 disks in the system. The EDSFF backplane is a 1U in height designed supporting state-of-the-art supports 8 pcs of EDSFF_E1.S SSD up to GEN5 through MCIO 8i (Mini Cool Edge IO) interfaces. The MCIO 8i connector could connect to NVMe HBA/RAID or PCIe Retimer Card that supports it.

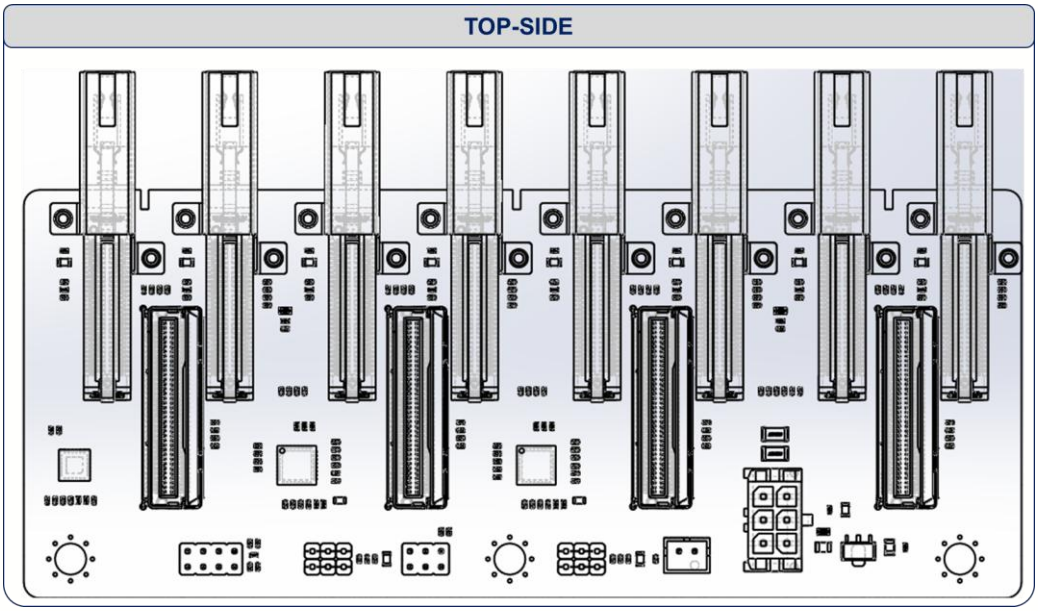
Basically, the 4 pcs of MCIO 8i connectors can support up to 8 EDSFF_E1.S SSD. 8 of the disk slots are the so called EDSFF_E1.S SSD via MCIO 8i connectors.

On backplane offer VRM with 2*3-Pin 12V (18A) DC input provide up to 3.3V (400mA) on board to satisfy the power needs of fully loaded for disk drives.

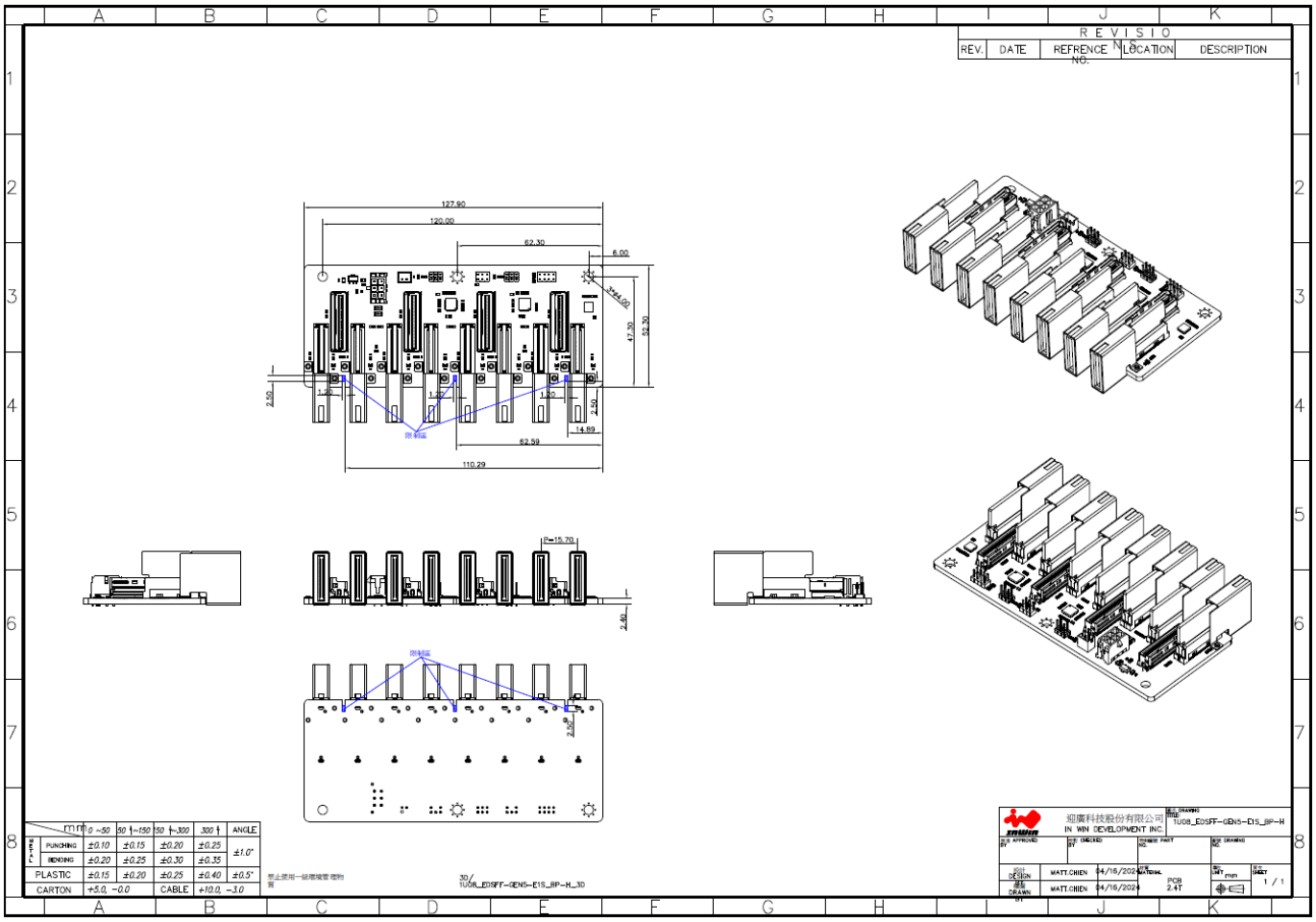
For disk bays management, the backplane supports supports UBM(Universal Backplane Management) for NVME disks activity and status indication through MCIO connections.

Physical Outlook

Diagram



Mechanical



Hardware Specification

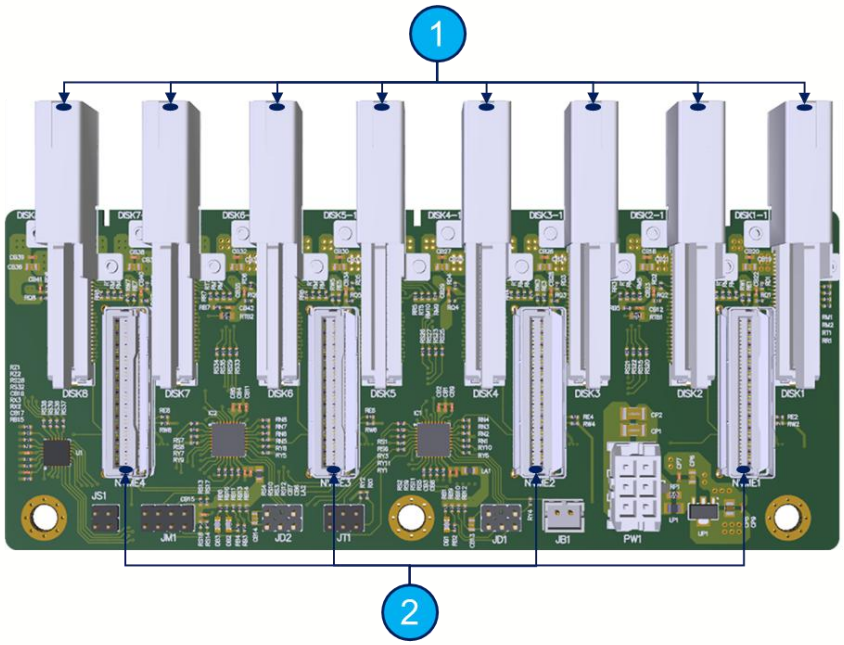
HOST Interface ： MCIO 8i

Hard Disk (SSD) Interface ： EDSSF-x4(1C)

- Indicator ： @E1.S SSD Front Panel
  - Dual color(Blue/Amber) LED D1~D8 for Hard Disk Drive Status (Fail/Locate)
  - Power/Activity LED: Green (When HDD is Access)
  - Fail/Locate LED : Amber (When HDD Fail or Locate)
  - Vender default : Blue
- Environment Control :
  - Temperature Sensor (RTB1/RTB2) Monitor HDD bay inside temperature.
- High Speed Connector
  - MCIO 8i Connector *4 (NVME1~NVME4)
    - All the MCIO 8i connectors(NVME1~NVME4) are directly wired to the E1.S 56-pin connectors(DISK1~DISK8).
  - E1.S 56Pin Connector *8 (DISK1~DISK8) for E1.S SSD.
- .Power Connector/Signal Control Header：
  - P3.0mm 2*3Pin Power Connector*1 (PW1 [+12V]).
  - JM1 SMBUS Connector for external BMC SMBUS control function.
  - JT1 Headers for UBM MODE & Test Mode Selection.
  - JD1/JD2 Header for Programming MCU Firmware.

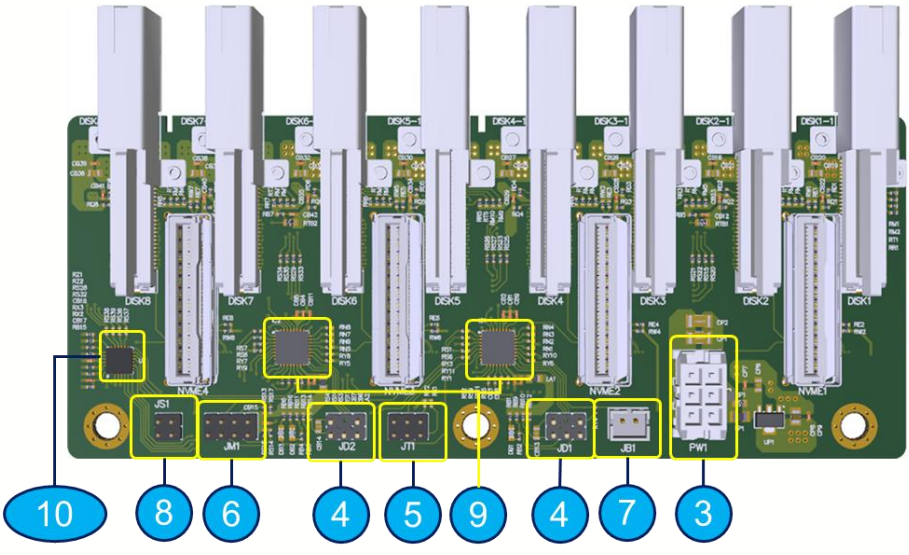
Host and Function Connector Location

TOP View – Host & Device Connector Location



No	Description	No	Description
1	Host facing interface : NVME1~NVME8	2	Device facing interface (E1.S) : DISK1~DISK8

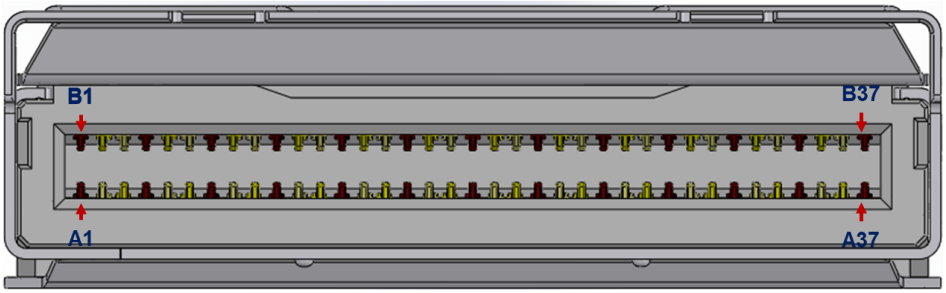
TOP View – Function Connector Location



No	Description	No	Description
3	Main Power Connector ： PW1	7	M/S Communication Connector : JB1
4	Firmware Programming Header ： JD1~JD2	8	
5	Multi-Function Selection : JT1	9	Micro-controller-Master : IC1
6	BMC_SMBUS Connector : JM1	10	Micro-controller-Slave1~2 : IC2~IC3

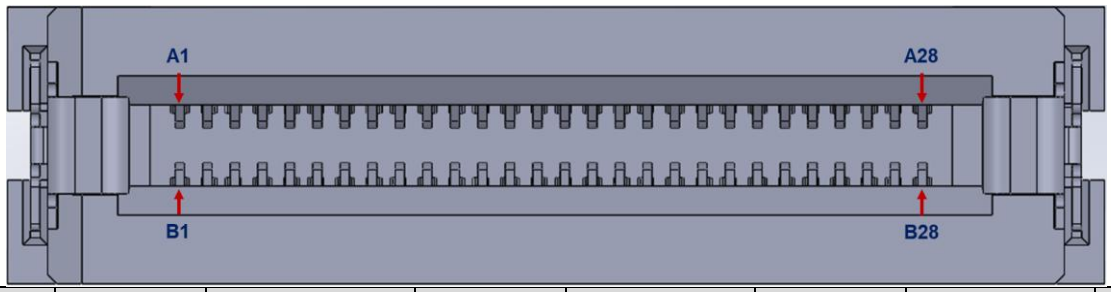
Connector Pin Definitions.

NVME1~NVME4

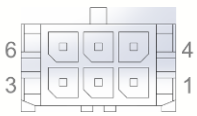


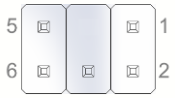
Signal Name	Pin No.	Signal Name	Pin No.	Signal Name	Pin No.	Signal Name	Pin No.
PET0_[p/n]	B2/B3	PET1_[p/n]	B5/B6	PET2_[p/n]	B14/B15	PET3_[p/n]	B17/B18
PER0_[p/n]	A2/A3	PER1_[p/n]	A5/A6	PER2_[p/n]	A14/A15	PER3_[p/n]	B17/B18
PET4_[p/n]	B20/B21	PET5_[p/n]	B23/B24	PET6_[p/n]	B32/B33	PET7_[p/n]	B35/B36
PER4_[p/n]	A20/A21	PER5_[p/n]	A23/A24	PER6_[p/n]	A32/A33	PER7_[p/n]	A35/A36
PCEI_GND	B1/B4/B7/B13/B16/B19/B22/B25/B31/B34/B37/A1/A4/A7/A13/A16/A19/A22/A25/A31/A34/A37						
BT_TYPE_A/B	B8/B26	CWAKE#_A/B	B9/B27	RefClk[p/n]_A	B11/B12	RefClk[p/n]_B	B29/B30
SMB_CLK_A	A8	SMB_DAT_A	A9	PERST#_A/B	A11/A29	SB_GNDA	A10/A28
SMBCLK_B	A26	SMBDAT_B	A27	CPRSNT#_A/B	A12/A30	SB_GNDB	B10/B28

DISK1~DISK8



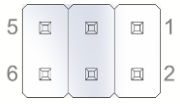
Signal Name	Pin No.	Signal Name	Pin No.	Signal Name	Pin No.	Signal Name	Pin No.
+12V	B1/B2/B3/B4/B5/B6			PWR_GND	A1/A2/A3/A4/A5/A6		
PET0_[p/n]	B18/B17	PET1_[p/n]	B22/B21	PET2_[p/n]	B25/B24	PET3_[p/n]	B27B26
PER0_[p/n]	A18/A17	PER1_[p/n]	A22/A21	PER2_[p/n]	A25/A24	PER3_[p/n]	A27/A26
PCEI_GNDA	A13/A16/A19/A22/A25/A28			PCEI_GNDB	B13/B16/B19/B22/B25/B28		
SMB_Clock	A7	MFG	B7	PERST1	A11	3.3V_AUX	B11
SMB_Data	A8	RFU	B8	PRSNT0	A12	PWRDIS	B12
SMRST	A9	DualPortEn	B9	SB_GND	A13	SB_GND	B13
LED	A10	PERSTN	B10	RefClk1[p/n]	A14/A15	RefClk0[p/n]	B14/B15

PW1	Power 2*4-Pin Connector	
	PIN #	Definition
	1~3	Ground
	4~6	+12V

JD1~JD2	Firmware Programming Header			
	PIN #	Definition	PIN No#	Definition
	1	VCC	2	ICE_CLK
	3	#Key	4	ICE_DATA
	5	Ground	6	ICE_RST

JM1	BMC_SMBUS Connector			
	PIN #	Definition	PIN #	Definition
	1	VCC	2	VCC
	3	Clock1	4	Clock2
	5	Data1	6	Data2
	7	GND	8	GND

JB1	M/S Communication Connector	
	PIN #	Definition
	1	EXT_SYNC1
	2	GND

JT1	Multi-Function Header			
	PIN #	Definition	PIN #	Definition
	1	UBM MODE	2	BP_NO_SEL1
	2	MODE_SEL	4	BP_NO_SEL2
	3	TSET_MODE	6	BP_NO_SEL3
JT1 Function Description: Pin#1-Pin#3 Short for UBM Mode. Pin#3-Pin#5 Short for TEST Mode Floating : VPP/SHP Mode			JT1 Function Description: Pin#2-Pin#4 Short for BP1. Pin#4-Pin#6 Short for BP2 Pin#4-Pin#6 Open for BP3	

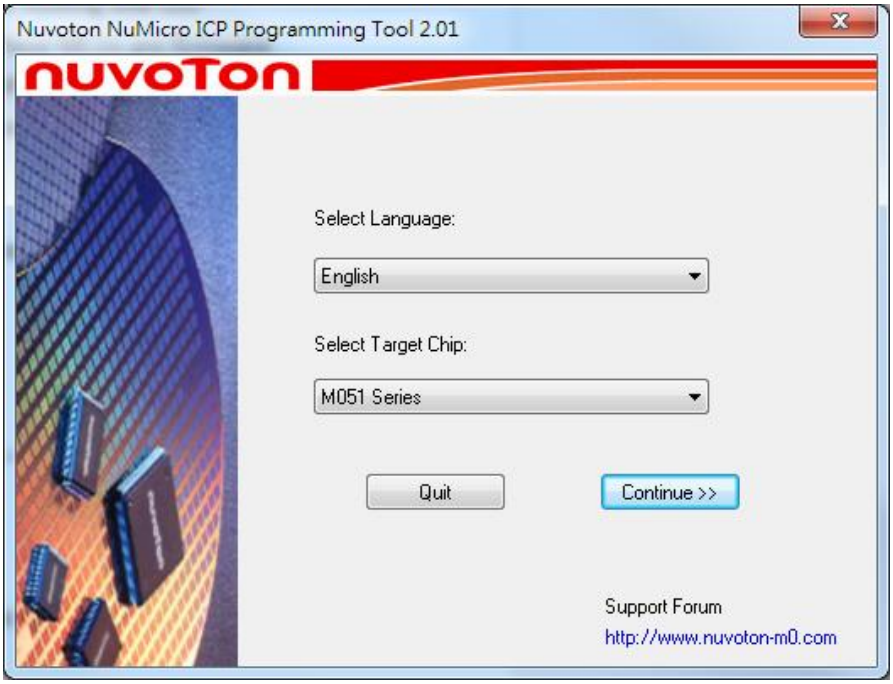
JS1	Multi-Function Header			
	PIN #	Definition	PIN #	Definition
	1	GND	2	SMB_ADDR0
	3	GND	4	SMB_ADDR0
JS1 Function Description: Pin#1-Pin#2 Short & Pin#3-Pin#4 Short for BP1- SMB_ADDR = 70H Pin#1-Pin#2 Open & Pin#3-Pin#4 Short for BP2- SMB_ADDR = 71H Pin#1-Pin#2 Short & Pin#3-Pin#4 Open for BP3- SMB_ADDR = 72H				

Firmware Upgrade

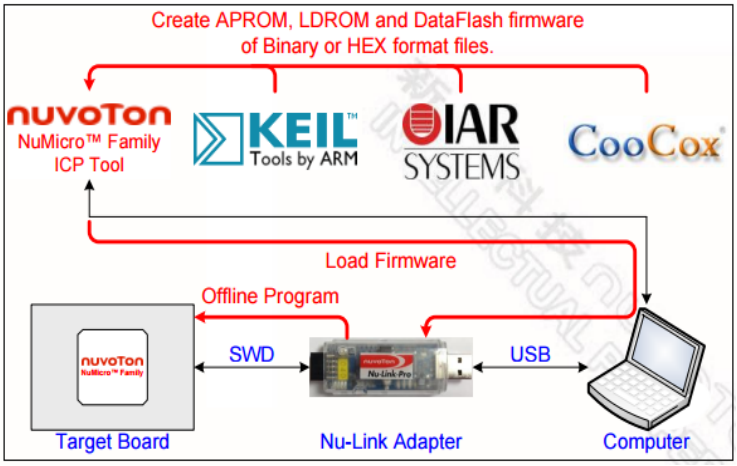
The passive backplanes are planted Nuvoton M482 series MCUs for hosting disk LED indication, Fan speed control and system fail alarm. These MCUs are preprogrammed in manufacturing. In most cases, the MCUs are not required to reprogram unless there is issue needed to fix.

How to upgrade firmware?

1. Require Nuvoton ARM Cortex-M0 programming tool. Nu-Me or Nu-Link and install Nuvoton ICP Programming tool software.

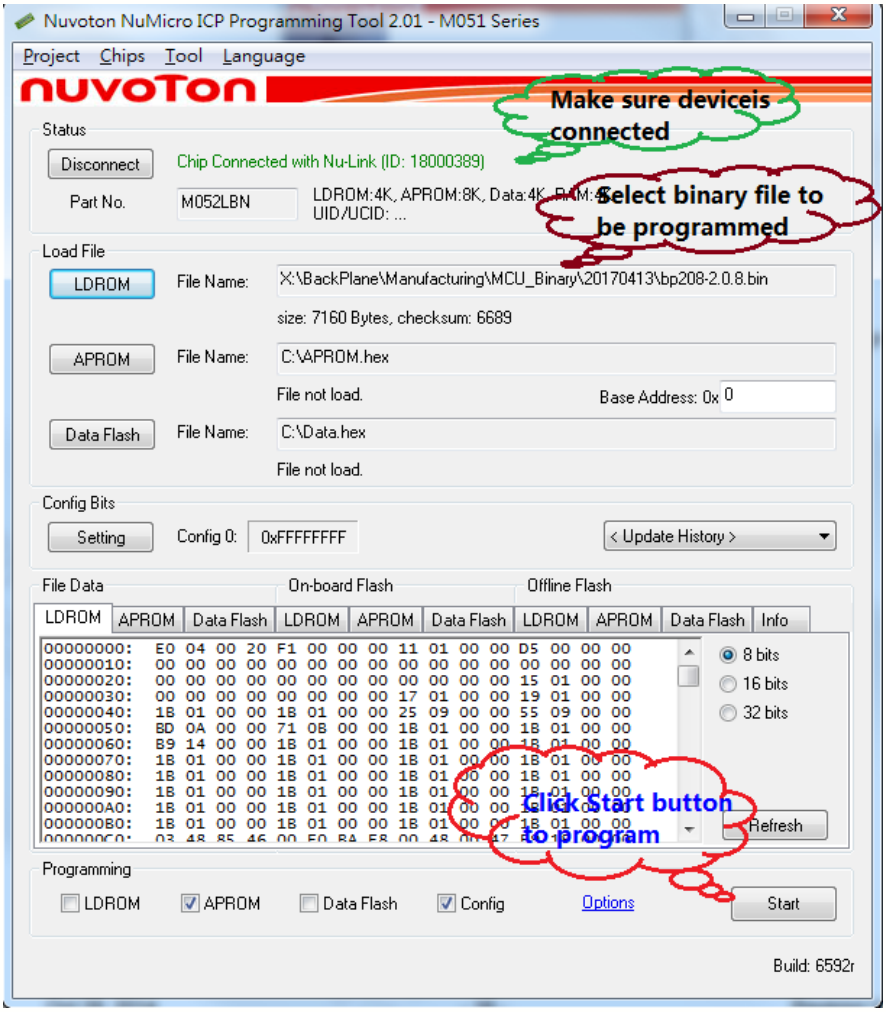


2. Connect Nu-Link USB end to a host and the SWD end to Backplane ICE connector for each MCU.



3. Make sure device is connected and select the binary file being programmed and then

click on Start button to program firmware.



4. Please refer to http://www.nuvoton.com/resource-files/NuLink_Adapter_User_Manual_EN_V1.01.pdf for more details.