EDSFF-E3.S GEN5 BP
USER'S MANUAL

P/N : 2RAKVI016800

Model：2U12-EDSFF-E3.S BP-H -GEN5 MODULE

Version: V1.0

Revision History

Version	Changes	Date
V1.0	Official Release	2025/03/15

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Overview

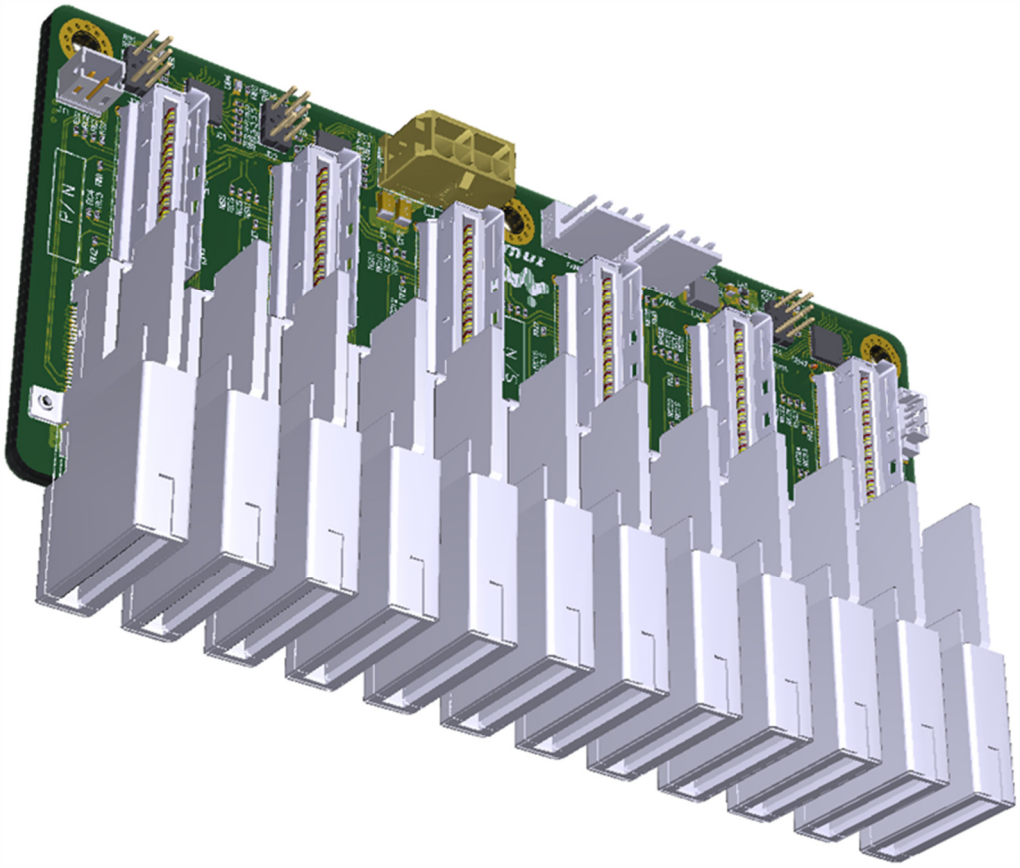
The backplane is a high performance economical solution for users who has sufficient MCIO host ports on MB or RAID/HBA to accommodate 12 disks in the system. The EDSFF backplane is a 2U in height designed supporting state-of-the-art supports 12 pcs of EDSFF_E3.S SSD up to GEN5 through MCIO 8i (Mini Cool Edge IO) interfaces. The MCIO 8i connector could connect to NVMe HBA/RAID or PCIe Retimer Card that supports it.

Basically, the 6 pcs of MCIO 8i connectors can support up to 12 EDSFF_E3.S SSD. 12 of the disk slots are the so called EDSFF_E3.S SSD via MCIO 8i connectors.

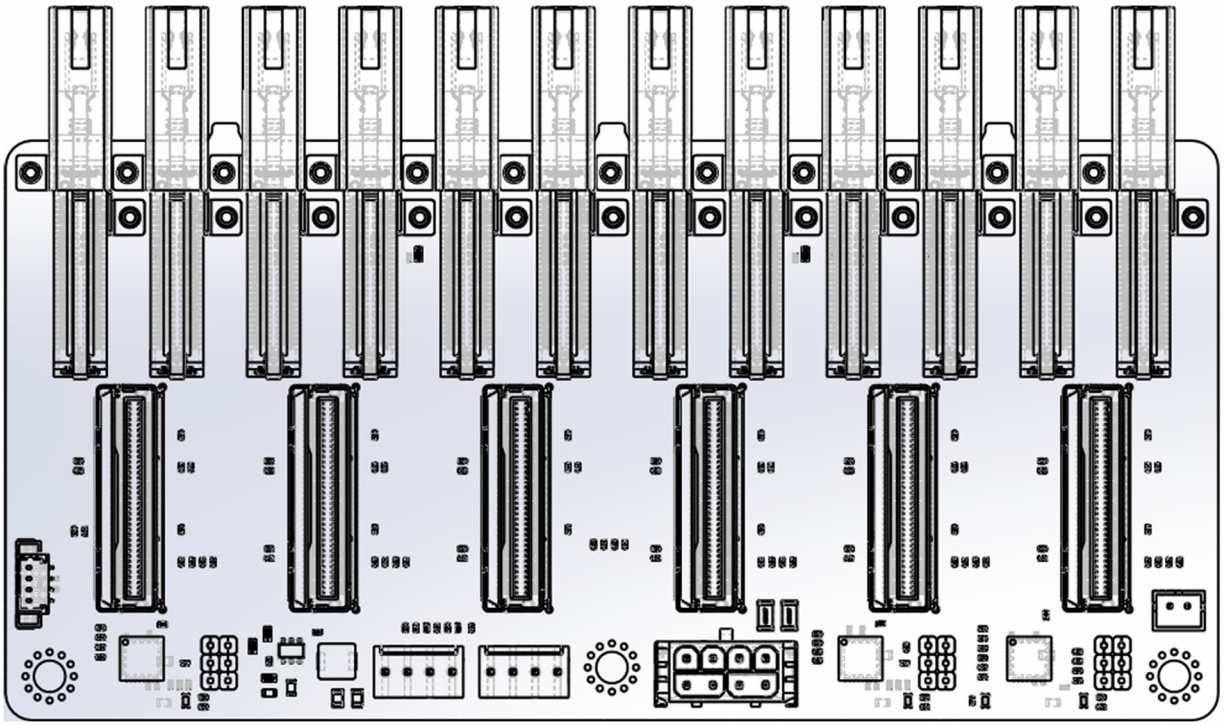
On backplane offer VRM with 2*4-Pin 12V (24A) DC input provide up to 3.3V (400mA) on board to satisfy the power needs of fully loaded for disk drives.

These devices are designed to connect via a PCI-E connector, utilizing the latest PCI-E technology and specifications.

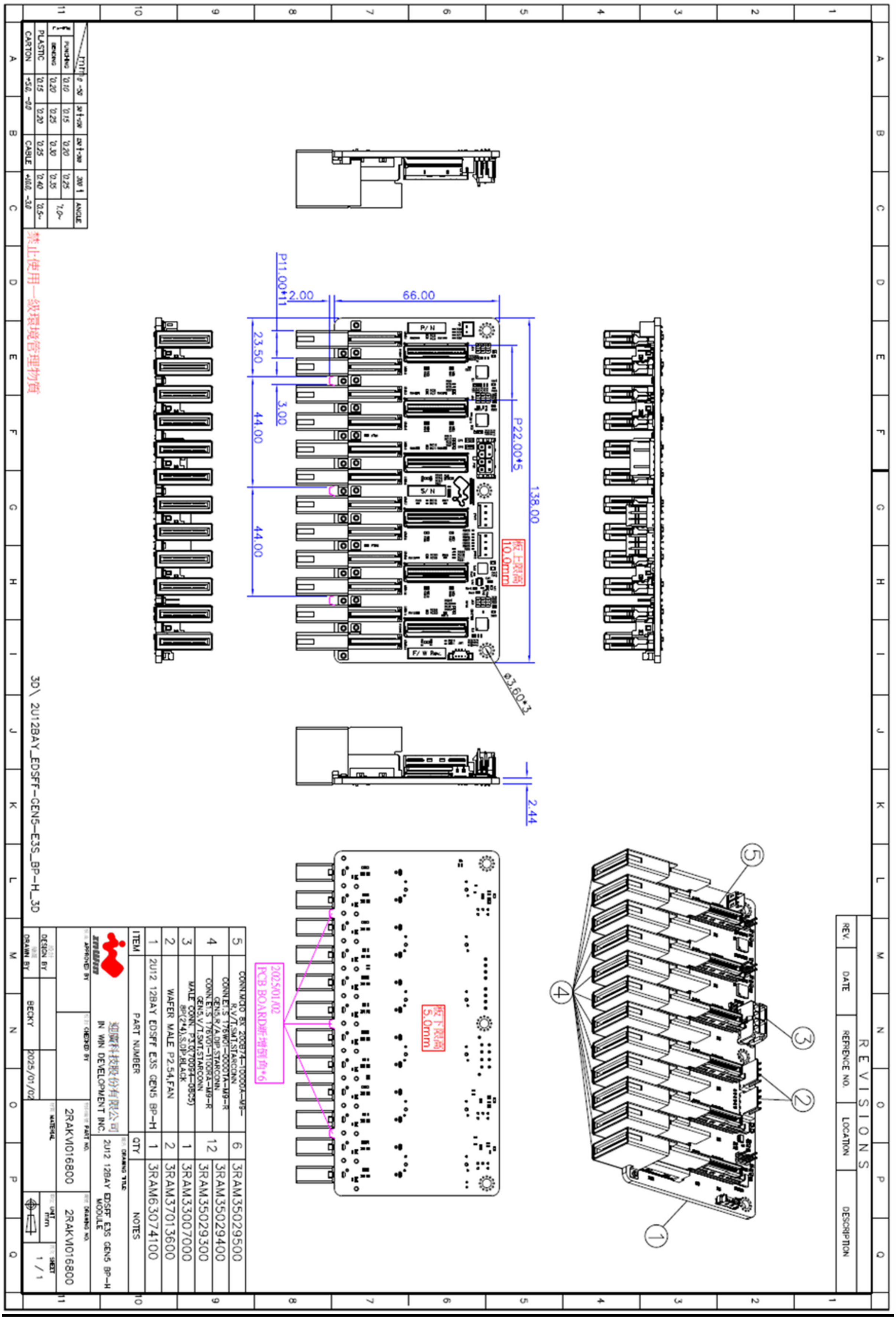
Physical Outlook



Diagram



Mechanical


66.00
2.00
23.50
3.00
44.00
44.00
138.00
2.44
2U12 12BAY EDSFF E3S GEN5 BP-H
2RAKVI016800
BECKY
2025/01/02

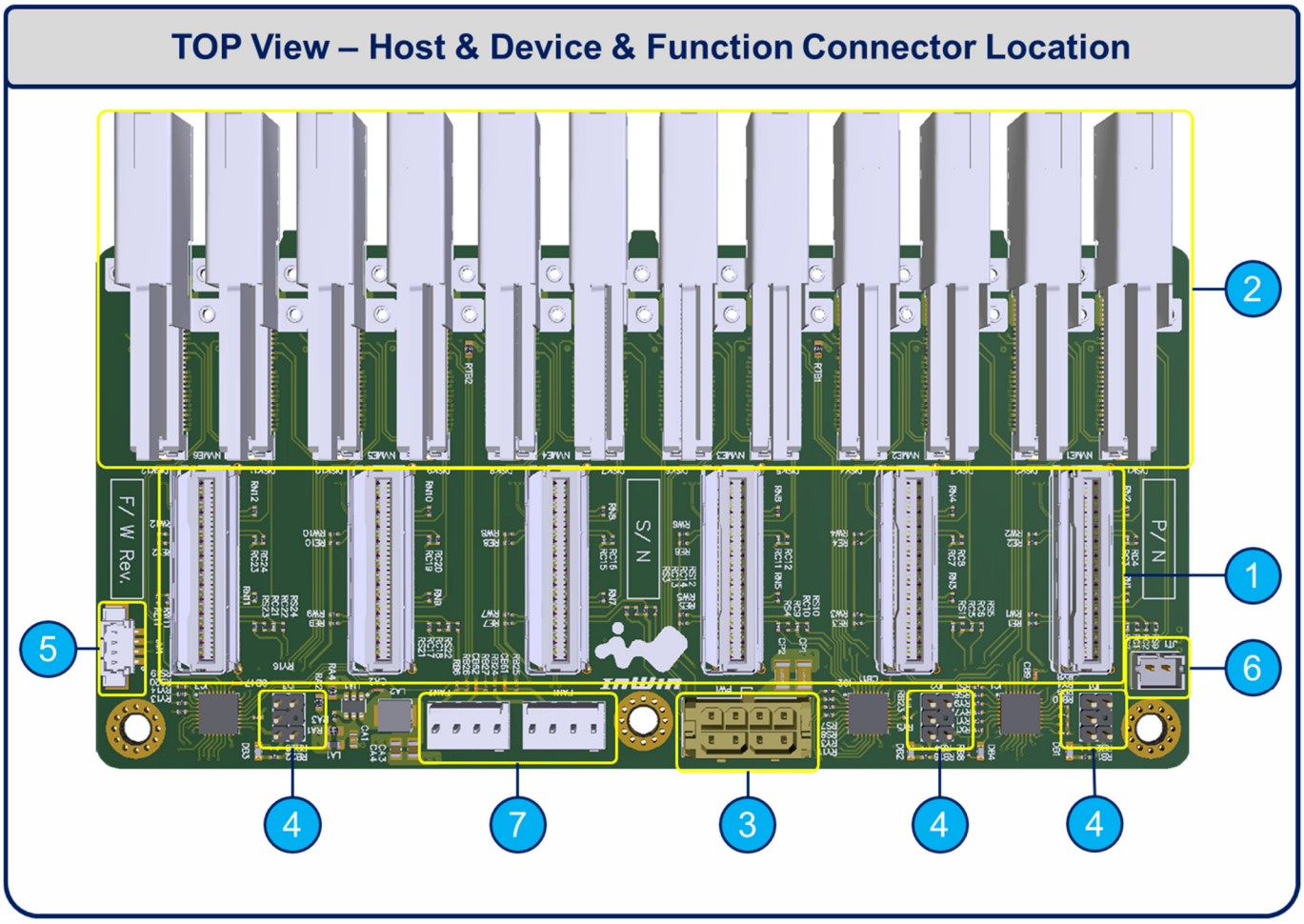
Hardware Specification

HOST Interface ： MCIO 8i

Hard Disk (SSD) Interface ： EDSSF-x4(1C)

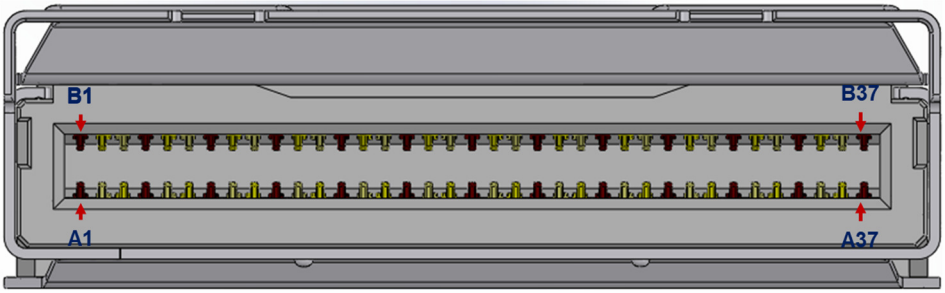
- Indicator ： @E3.S SSD Front Panel
  - Dual color(Blue/Amber) LED D1~D12 for Hard Disk Drive Status (Fail/Locate)
  - Power/Activity LED: Green (When HDD is Access)
  - Fail/Locate LED : Amber (When HDD Fail or Locate)
  - Vender default : Blue
- Environment Control :
  - PWM FAN Connector (FAN1~FAN2) for Cooling system.
  - Temperature Sensor (RTB1/RTB2) Monitor HDD bay inside temperature.
- High Speed Connector
  - MCIO 8i Connector *3 (NVME1~NVME6)
    - All the MCIO 8i connectors(NVME1~NVME6) are directly wired to the E3.S 56-pin connectors(DISK1~DISK12).
  - E1.S 56Pin Connector *12 (DISK1~DISK12) for E3.S SSD.
- .Power Connector/Signal Control Header：
  - P3.0mm 2*4Pin Power Connector*1 (PW1 [+12V]).
  - JM1 SMBUS Connector for external BMC SMBUS control function.
  - JT1 Headers for UBM MODE & Test Mode Selection.
  - JD1/JD2/JD3 Header for Programming MCU Firmware.
  - JS1 Header for BP No. Selection

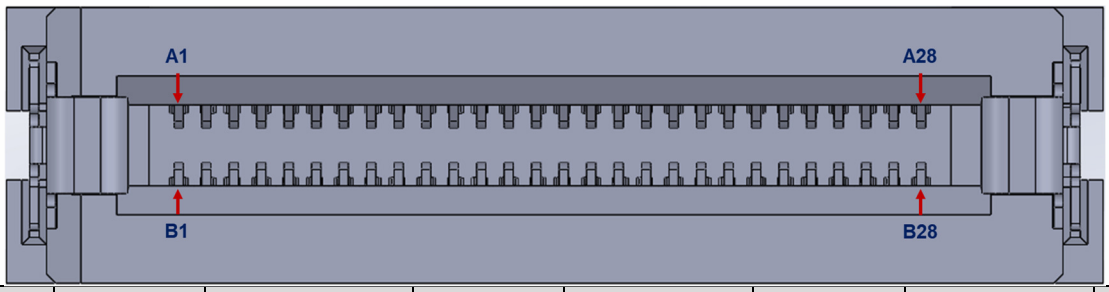
Host and Function Connector Location

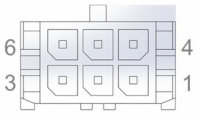


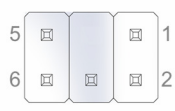
No	Description	No	Description
1	Host facing interface : NVME1~NVME8	5	BMC_SMBUS Connector : JM1
2	Device facing interface (E3.S) : DISK1~DISK12		
3	Main Power Connector ： PW1	6	M/S Communication Connector : JB1
4	Firmware Programming Header:JD1~JD3	7	FAN Connector : FAN1~FAN2

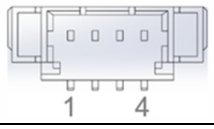
Connector Pin Definitions.

NVME1~NVME4							
							
Signal Name	Pin No.	Signal Name	Pin No.	Signal Name	Pin No.	Signal Name	Pin No.
PET0_[p/n]	B2/B3	PET1_[p/n]	B5/B6	PET2_[p/n]	B14/B15	PET3_[p/n]	B17/B18
PER0_[p/n]	A2/A3	PER1_[p/n]	A5/A6	PER2_[p/n]	A14/A15	PER3_[p/n]	B17/B18
PET4_[p/n]	B20/B21	PET5_[p/n]	B23/B24	PET6_[p/n]	B32/B33	PET7_[p/n]	B35/B36
PER4_[p/n]	A20/A21	PER5_[p/n]	A23/A24	PER6_[p/n]	A32/A33	PER7_[p/n]	A35/A36
PCEI_GND	B1/B4/B7/B13/B16/B19/B22/B25/B31/B34/B37/A1/A4/A7/A13/A16/A19/A22/A25/A31/A34/A37						
BT_TYPE_A/B	B8/B26	CWAKE#_A/B	B9/B27	RefClk[p/n]_A	B11/B12	RefClk[p/n]_B	B29/B30
SMB_CLK_A	A8	SMB_DAT_A	A9	PERST#_A/B	A11/A29	SB_GNDA	A10/A28
SMBCLK_B	A26	SMBDAT_B	A27	CPRSNT#_A/B	A12/A30	SB_GNDB	B10/B28

DISK1~DISK8							
							
Signal Name	Pin No.	Signal Name	Pin No.	Signal Name	Pin No.	Signal Name	Pin No.
+12V	B1/B2/B3/B4/B5/B6			PWR_GND	A1/A2/A3/A4/A5/A6		
PET0_[p/n]	B18/B17	PET1_[p/n]	B22/B21	PET2_[p/n]	B25/B24	PET3_[p/n]	B27B26
PER0_[p/n]	A18/A17	PER1_[p/n]	A22/A21	PER2_[p/n]	A25/A24	PER3_[p/n]	A27/A26
PCEI_GNDA	A13/A16/A19/A22/A25/A28			PCEI_GNDB	B13/B16/B19/B22/B25/B28		
SMB_Clock	A7	MFG	B7	PERST1	A11	3.3V_AUX	B11
SMB_Data	A8	RFU	B8	PRSNT0	A12	PWRDIS	B12
SMRST	A9	DualPortEn	B9	SB_GND	A13	SB_GND	B13
LED	A10	PERSTN	B10	RefClk1[p/n]	A14/A15	RefClk0[p/n]	B14/B15

PW1	Power 2*4-Pin Connector	
	PIN #	Definition
	1~3	Ground
	4~6	+12V

JD1~JD3	Firmware Programming Header			
	PIN #	Definition	PIN No#	Definition
	1	VCC	2	ICE_CLK
	3	#Key	4	ICE_DATA
	5	Ground	6	ICE_RST

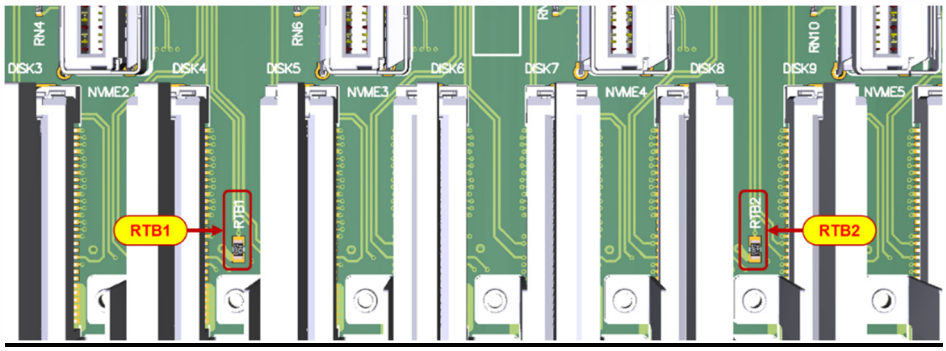
JB1	EEPROM Programing	
	PIN #	Definition
	1	VCC
	2	SMB_CLK
	3	SMB_DAT
	4	Ground

JB1	M/S Communication Connector	
	PIN #	Definition
	1	EXT_SYNC1
	2	GND

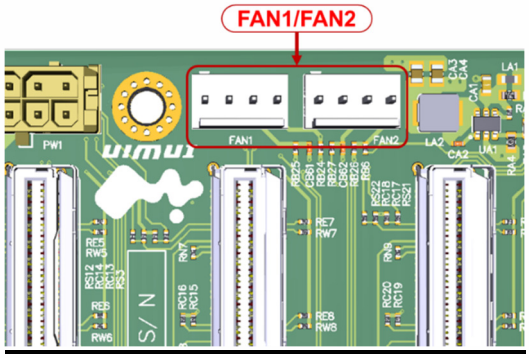
FAN1~FAN2	FAN 4-Pin Connector	
	PIN #	Definition
	1	Ground
	2	+12V
	3	Tachometer
	4	PWM Output

Smart Fan Control

IN WIN's Backplane is implemented Smart Fan Control feature by automatically detecting the existences of the Fan Modules and intelligently control the Fan RPM per the system temperature being detected by two thermal sensors (RTB1/RTB2) on the backplane.

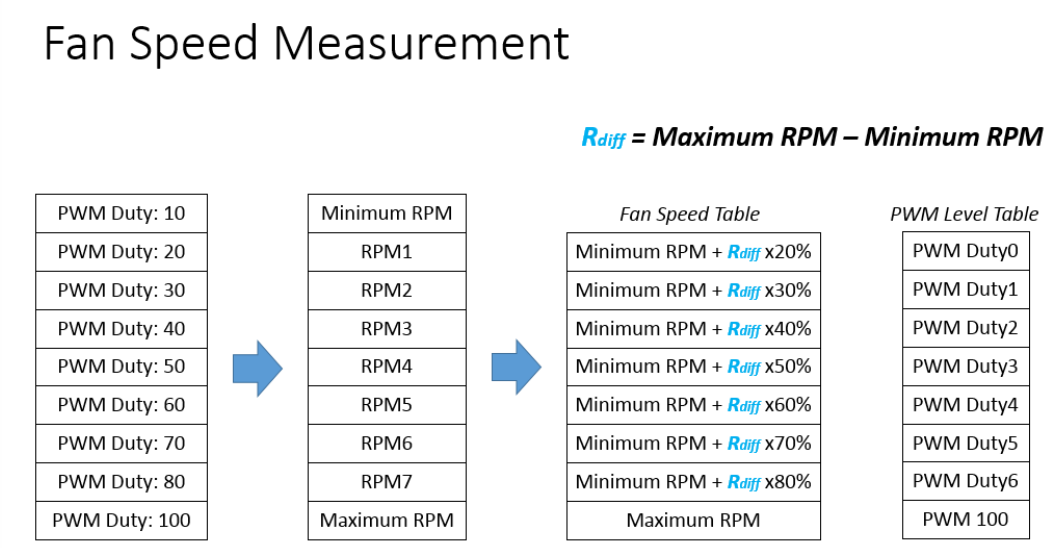


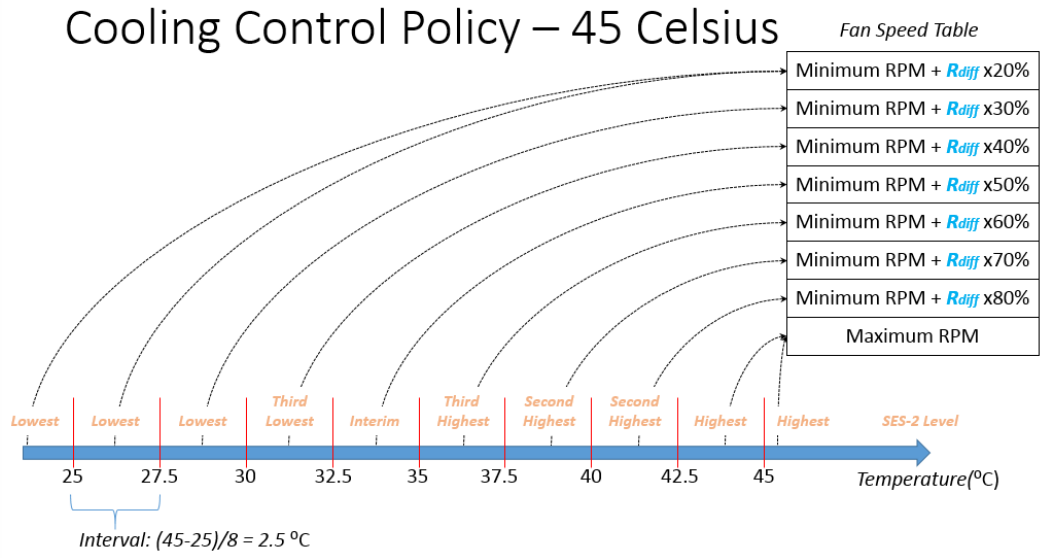
Thanks to Smart Fan Control feature the Fan connectors (FAN1/FAN2) on backplane support wide variety of PWM driven Fan modules being used in the enclosure.



How it works?

1. Fan module auto-calibration triggered in every system boot. The thermal profile would then be recorded and used until next reboot.
2. Backplane starts fan calibration and calculates the corresponding PWM duty cycle for each level. There are totally 8 speed levels to be sensed and used until next system boot.
3. The 8 levels of fan speed are mapped to the temperature readings detected by thermistor spreading from 25 to 45 ℃ in 3.75 degree C step.
4. In normal operation, when the system temperature changes to next level, the fan module would change speed accordingly. And, the Fan failure alarm would be triggered when the RPM of the Fan module is dropped lower than 75% of its expected speed.
5. The fan module calibration and thermal profile are as below.
6. When an external PWM source joins, the output PWM duty is determined by comparing the internal calculated PWM and external PWM and then select whichever is higher as the output PWM to the fan modules.



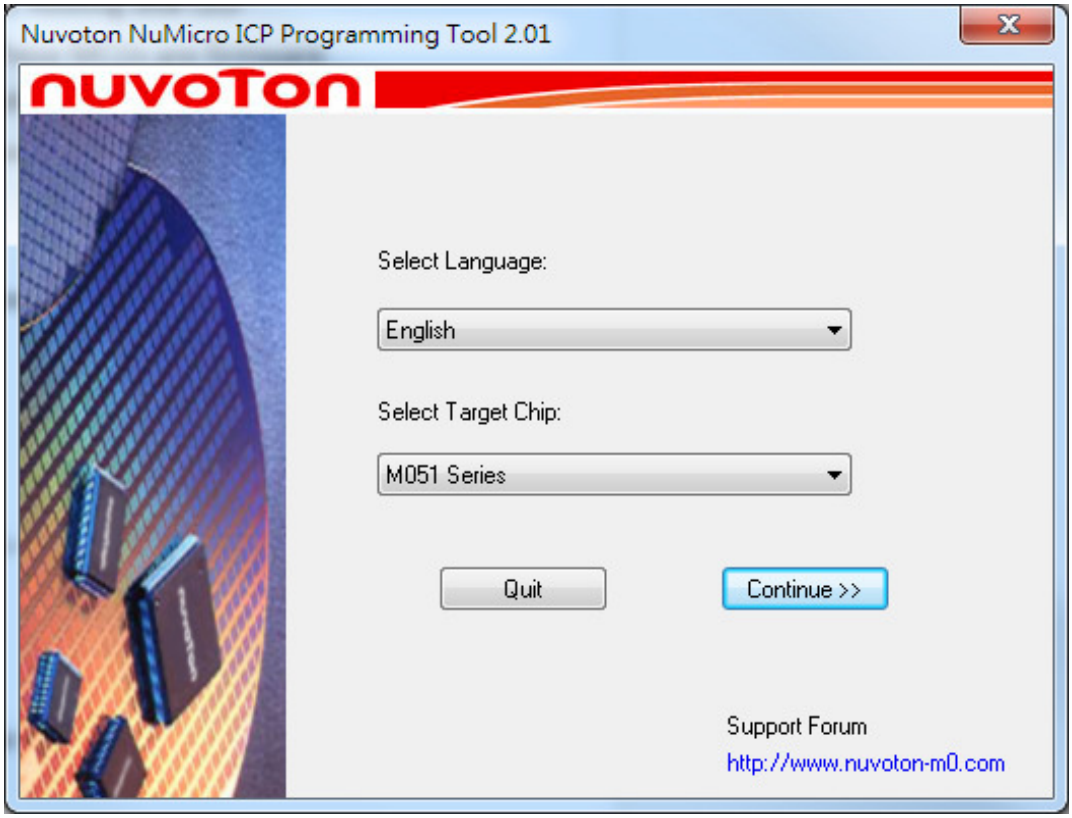


Firmware Upgrade

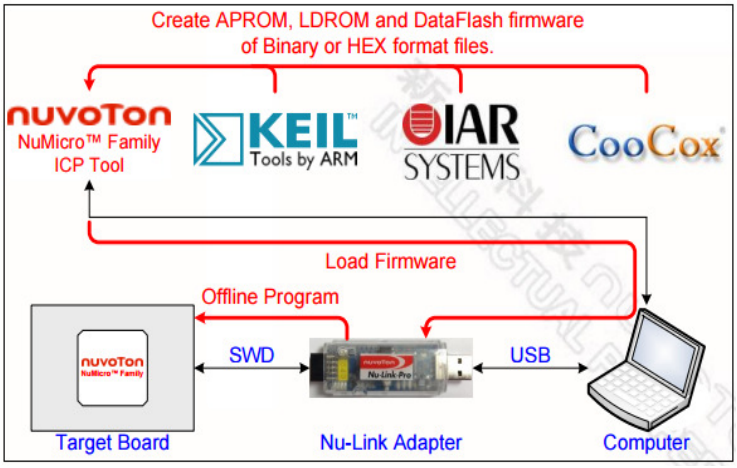
The passive backplanes are planted Nuvoton M482 series MCUs for hosting disk LED indication, Fan speed control and system fail alarm. These MCUs are preprogrammed in manufacturing. In most cases, the MCUs are not required to reprogram unless there is issue needed to fix.

How to upgrade firmware?

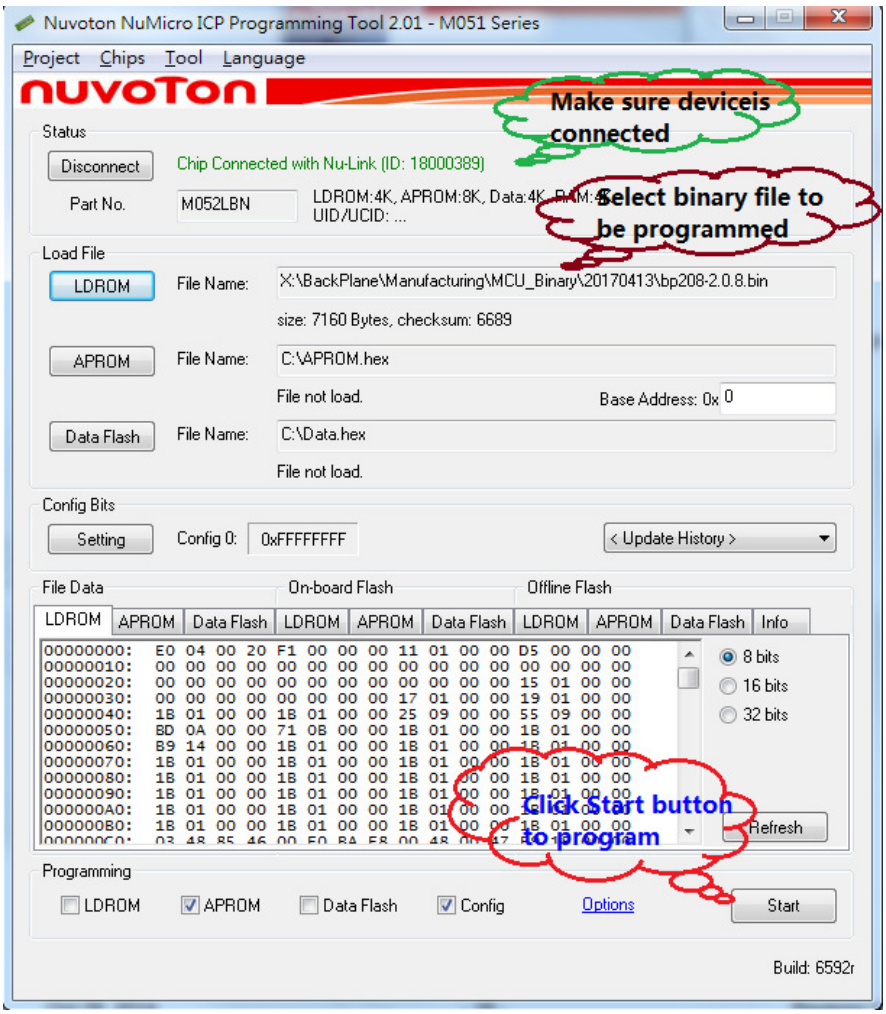
1. Require Nuvoton ARM Cortex-M0 programming tool. Nu-Me or Nu-Link and install Nuvoton ICP Programming tool software.



2. Connect Nu-Link USB end to a host and the SWD end to Backplane ICE connector for each MCU.



3. Make sure device is connected and select the binary file being programmed and then click on Start button to program firmware.



4. Please refer to http://www.nuvoton.com/resource-files/NuLink_Adapter_User_Manual_EN_V1.01.pdf for more details.